UNITED STATES PATENT AND TRADEMARK OFFICE

A

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/954,638	09/14/2001	Christophe Lauga	851963.401	6890

500 7590 08/08/2005

SEED INTELLECTUAL PROPERTY LAW GROUP PLLC
701 FIFTH AVE
SUITE 6300
SEATTLE, WA 98104-7092

EXAMINER	
KERVEROS, JAMES C	

ART UNIT	PAPER NUMBER
2133	

DATE MAILED: 08/08/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/954,638	LAUGA, CHRISTOPHE	
	Examiner	Art Unit	
	JAMES C. KERVEROS	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *01 June 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *9/14/01* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 6/1/2005 has been entered.

This is a Non-Final Office Action in response to RCE and AMENDMENT filed 6/1/2005. Claims 1-22 were rejected in the prior Office Action. Claims 23-25 are new. Claims 1-25 are pending.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-5, 8-20 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komoike (U.S. Patent N0. 6,094,736) in view of Kim et al. (U.S. Patent No. 6,148,426).

Regarding independent Claims 1, 10, Komoike substantially discloses a (semiconductor chip 1) comprising a plurality of combinational logic components (CPU or logic circuit 4), a memory (DRAM 2), and a testing arrangement for configuring the memory prior to testing the combinational logic using a plurality of selectors 8 and scan flip flops 9 mounted on the semiconductor chip (see Abstract and Figures 1-5), the arrangement, comprising:

Test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the wiring group 7, which are transferred through the input terminals A to E and then stored in the DRAM 2.

A switching arrangement (selector group 8), which is controlled by a control signal through the wiring 6, for selectively switching the memory DRAM 2 input terminals A to E to receive data from the combinational logic (terminals A to E) in the (CPU or the logic circuit 4) or (test patterns), which are transferred from the upper four scan flip flops 9 and then stored in the DRAM 2.

The switching arrangement (selector group 8) and data generator are arranged for the data generator to input the selected (test patterns) to the memory DRAM 2, during the test operation of the DRAM 2, which is executed before the normal mode, shown in Figure 1 and 2, (cols. 6 and 7, lines 55-67 and 1-50, respectively), described in a timing sequence next, as follows:

First, when the test operation of the DRAM 2 is performed, the level of a test mode signal is set to a high (H) level, which halts the signal transfer/receiving operation in a normal process.

Next, the semiconductor integrated circuit device inputs test to the DRAM 2. Following this, test patterns are read from the DRAM 2 as a test results and are compared with the original test patterns in order to detect whether or not the DRAM 2 has any fault.

After this, the test mode signal is set to a low (L) level so that the signal transfer/receiving operation in the normal process may be performed.

A testing circuit, in Figure 4, for testing the combinational logic components (CPU or a logic circuit 4), after the data generator through the wiring group 7 has input the test patterns to the memory, namely after the test operation of the DRAM 2, as follows:

As shown in Figure 5E, the scan mode signal SM is set to the L level, and parallel output data items to be used for the target test circuit X are then transferred from the flip flops (L, M, and N) 9 onto the pass designated by the solid line according to the clock signal. Next, as shown in FIG. 5F, when the scan mode signal SM is set to the H level, the output data items from the target test circuit X are transferred to the flip flops (L, M, and N) 9 in order through the pass designated by the solid lines. Thereby, serial scan output (SO) data items as the test result are transferred to an external device (omitted from the drawings) through the terminal for the scan output SO.

Komoike does not explicitly disclose "a data generator being internal to the integrated circuit".

However, in an analogous art, Kim discloses a data generator 103, internal to a semiconductor device using a SRAM BIST circuit 100 implemented in connection with

memory test processes, Figure 1, which generates data to be written to the memory block 200 under test (i.e., the SRAM) and to also generate comparison data. During test, the comparison data is compared to data written to an addressed location of the memory block 200 to determine whether data can successfully be written to and read from the memory 200.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a BIST circuit having a data generator as taught by Kim in the semiconductor chip of Komoike, for the purpose of generating data to verify a memory under test, by determining whether data can successfully be written to and read from the memory under test using a SRAM BIST implementation in connection with the memory test processes. A person skilled in the art would have been motivated to incorporate a BIST circuit internal to the semiconductor chip having a data generator, since a BIST circuit provides advantages over other devices by reducing overall circuit size and complexity, thus resulting in further savings in size, complexity and cost (Kim, Col. 2, lines 55-62).

Regarding Claim 2, Komoike discloses the arrangement further comprising an enable input (scan mode signal SM, 6A, Figures 3 and 4), which controls the test pattern readout operation, thus preventing writing to the memory DRAM 2 during the read out of data pattern.

Regarding Claim 3, Komoike discloses test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the

wiring group 7, wherein the test patterns comprising address and data corresponding to address inputs of the memory DRAM 2.

Regarding Claim 4, Komoike discloses comprising an arrangement of multiplexers (selector group 8) for selectively switching the memory DRAM 2 input terminals A to E to receive data from the combinational logic (terminals A to E in the CPU or the logic circuit 4) or from the data generator (test patterns), which are transferred from the upper four scan flip flops 9 to the DRAM 2. Then, the DRAM 2 stores the parallel test patterns from the upper four scan flip flops 9 according to the clock signal.

Regarding Claim 5, Komoike discloses test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the wiring group 7, wherein the test patterns inherently comprising address and data corresponding to address inputs of the memory DRAM 2.

Regarding Claim 8, Komoike discloses a wrapper circuit including scan flip flops 9 formed corresponding to the selectors 8, for selectively preloading the memory DRAM 2 with serial test patterns from the scan flip flops 9.

Regarding Claim 9, Komoike discloses a wrapper circuit including scan flip flops 9 formed corresponding to the selectors 8, including a control signal (scan mode signal SM, 6A, Figures 3 and 4), which controls the test pattern readout operation, thus controlling the memory to behave as a ROM.

Regarding Claim 11, Komoike discloses a multiplexer (selector group 8) having one input coupled to the logic elements (CPU or the logic circuit 4) and another input

coupled to the data generator (test patterns) provided from an external device (omitted from the drawings) through the wiring group 7, and a control signal coupled to the control circuitry through the wiring 6, for selectively connecting the memory DRAM 2 to the logic elements or to the data generator, Figure 3.

Regarding Claims 12, 14, Komoike discloses loading into the memory array prior to testing of the semiconductor circuit, by inputting the selected (test patterns) to the memory DRAM 2, during the test operation of the DRAM 2, which is executed before the normal mode, shown in Figure 1 and 2, (cols. 6 and 7, lines 55-67 and 1-50, respectively), as described by the timing sequence in claim 1, above.

Regarding Claim 13, Komoike discloses test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the wiring group 7, wherein the test patterns comprising address and data corresponding to address inputs of the memory DRAM 2.

Regarding Claim 15, Komoike discloses test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the wiring group 7, wherein the test patterns inherently comprising address and data corresponding to address inputs of the memory DRAM 2.

Regarding Claims 16, 17 and 18, Komoike discloses writing test patterns selected based on the memory type such as DRAM2, which is tested the same way as a RAM or CAM memory, due to their equivalent functionality.

Regarding Claim 19, a wrapper circuit including scan flip flops 9 formed corresponding to the selectors 8, including a control signal (scan mode signal SM, 6A,

Figures 3 and 4), which controls the test pattern readout operation, thus controlling the memory to behave as a ROM.

Regarding independent Claim 20, Komoike substantially discloses a method of testing logic (CPU or logic circuit 4) in the same (semiconductor chip 1) as a memory DRAM 2, (see Abstract and Figures 1-5), comprising:

Switching a memory (DRAM 2 input terminals A to E) with a multiplexer (selector group 8) to receive input data, such as, address, data and control signals, from an external device, in a first state, Figure 21, which shows a semiconductor chip 1, a DRAM 2 mounted on the semiconductor chip and a wiring 3 having a plurality of lines through which test patterns are transferred from an external device (omitted from Figure 21) to the DRAM 2.

During the second state (internal to the semiconductor chip 1):

Writing the selected bit pattern into memory DRAM 2, using a switching arrangement (selector group 8), which is controlled by a control signal through the wiring 6, for selectively switching the memory DRAM 2 input terminals A to E to receive data from the combinational logic (terminals A to E in the CPU or the logic circuit 4) or from the data generator (test patterns), which are transferred from the upper four scan flip flops 9 to the DRAM 2. Then, the DRAM 2 stores the parallel test patterns from the upper four scan flip flops 9 according to the clock signal.

Inputting selected data into the logic (CPU or logic circuit 4) to be tested, using testing circuit, in Figure 4, for testing the combinational logic components (CPU or a

logic circuit 4), after the data generator through the wiring group 7 has input the test patterns to the memory, namely after the test operation of the DRAM 2, as follows:

As shown in Figure 5E, the scan mode signal SM is set to the L level, and parallel output data items to be used for the target test circuit X are then transferred from the flip flops (L, M, and N) 9 onto the pass designated by the solid line according to the clock signal. Next, as shown in FIG. 5F, when the scan mode signal SM is set to the H level, the output data items from the target test circuit X are transferred to the flip flops (L, M, and N) 9 in order through the pass designated by the solid lines. Thereby, serial scan output (SO) data items as the test result are transferred to an external device (omitted from the drawings) through the terminal for the scan output SO.

Transferring signals from (terminals A to E) of the (CPU or logic circuit 4) to be tested to the (input terminals A to E) of the memory DRAM 2 and from the (output terminals F to J) of the memory DRAM 2 to the (terminals F to J) of the (CPU or logic circuit 4) to be tested.

Komoike does not explicitly disclose, "generating an address with the internal address counter for determining the address at which data will be written, coupling an output of the internal address counter with an input of the internal data generator, generating a selected bit pattern with the internal data generator based upon the value of the internal address counter".

However, in an analogous art, Kim discloses a data generator 103 and an address generator 105 internal to a semiconductor device using a SRAM BIST circuit 100 implemented in connection with memory test processes, Figure 1. The data

generator 103 generates data to be written to the memory block 200 under test (i.e., the SRAM) and also generates comparison data. The address generator 105 generates the addresses of the locations of the memory block 200 being tested.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to incorporate a BIST circuit having a data and an address generator as taught by Kim in the semiconductor chip of Komoike, for the purpose of generating data and address to verify a memory under test, by determining whether data can successfully be written to and read from the memory under test using a SRAM BIST implementation in connection with the memory test processes. A person skilled in the art would have been motivated to incorporate a BIST circuit internal to the semiconductor chip having data and address generator, since a BIST circuit provides advantages over other devices by reducing overall circuit size and complexity, thus resulting in further savings in size, complexity and cost (Kim, Col. 2, lines 55-62).

Regarding Claim 23, placing the memory (DRAM 2) in a state that simulates a combinatorial logic function, designated as target test circuit Y, as shown in Figure 5.

Claims 24 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komoike (U.S. Patent N0. 6,094,736) in view of Beauchesne et al. (U.S. Patent No. 4,481,627).

Regarding independent Claim 24, Komoike substantially discloses a method of testing logic elements (CPU or logic circuit 4) that are in the same (semiconductor chip 1) as a memory DRAM 2, (see Abstract and Figures 1-5), comprising:

Inputting to the memory array DRAM 2 test patterns provided to the semiconductor chip 1 from an external device (omitted from the drawings) through the wiring group 7, which are transferred to the DRAM 2 through the input terminals A to E and then stored in the DRAM 2. The pattern being selected, using (selector group 8), which is controlled by a control signal through the wiring 6, for selectively switching the memory DRAM 2 input terminals A to E to receive data from terminals A to E in the (CPU or the logic circuit 4) or from the (test patterns), which are transferred from the upper four scan flip flops 9 to the DRAM 2. Then, the DRAM 2 stores the parallel test patterns from the upper four scan flip flops 9 according to the clock signal.

Setting the integrated circuit in logic test mode for testing logic (CPU or logic circuit 4) that is outside of the memory array DRAM 2, as shown in Figure 5E. The scan mode signal SM is set to the L level, and parallel output data items to be used for the target test circuit X are then transferred from the flip flops (L, M, and N) 9 onto the pass designated by the solid line according to the clock signal. Next, as shown in FIG. 5F, when the scan mode signal SM is set to the H level, the output data items from the target test circuit X are transferred to the flip flops (L, M, and N) 9 in order through the pass designated by the solid lines. Thereby, serial scan output (SO) data items as the test result are transferred to an external device (omitted from the drawings) through the terminal for the scan output SO.

Inputting signals from (terminals A to E) of the (CPU or logic circuit 4) to be tested to the (input terminals A to E) of the memory DRAM 2 and receiving from the (output terminals F to J) of the memory DRAM 2, as part of testing the (CPU or logic circuit 4). The memory acting as a portion of the logic circuit during the testing of the logic elements of the integrated circuit.

Komoike does not explicitly disclose configuring the memory array to operate as a combinatorial logic circuit for the input of signals and the output of signal based on the input.

However, in analogous art, Beauchesne discloses an embedded memory 150, which can be isolated from the combinatorial logic element 160 and tested by use of a memory test subsystem 110 either before or after the combinatorial logic elements are tested by a logic test subsystem, see Abstract and Figure 1.

It would have been obvious to a person having ordinary skill in the art at the time the invention was made to configure the memory array of Komoike by isolating the memory array from the combinatorial logic element as taught by Beauchesne, for the purpose of testing the combinatorial logic, since the memory can tested by the use of a memory test subsystem either before or after the combinatorial logic elements. A person skilled in the art would have been motivated to configure the memory by isolating the memory from the combinatorial logic element, since memory arrays embedded in electronic assemblies with other combinatorial logic can be tested to nearly the same precision as separately implemented or non-embedded memory arrays.

Regarding Claim 25, Komoike discloses sending signals serial input data (SI) via a scan chain (scan flip flops 9) between respective logic elements (target test circuits X and Y) being tested, as shown in Figure 5.

Claims 6, 7, 21 and 22 are rejected under 35 U.S.C. 103(a) as being unpatentable over Komoike (U.S. Patent N0. 6,094,736) in view of Kim et al. (U.S. Patent No. 6,148,426), and further in view of Rapoport (U.S. Patent No. 5,557,619).

Regarding Claims 6, 7, 21 and 22, the combined device of Komoike and Kim does not disclose a checkerboard pattern and wherein the pattern is so arranged that the RAM may be modeled as a simple combinational circuit.

However, Rapoport discloses a novel processor-based ABIST circuit, which can be programmed with a "read complement checkerboard pattern", to verify the functionality of memory unit 12. In addition Rapoport discloses conventional state machine based ABIST having combinational logic circuits to generate each hard-coded test pattern, (column 11, line 30-35). It would have been obvious to a person having ordinary skill in the art at the time the invention was made to use a checkerboard pattern and combinational logic circuits, as taught by Rapoport, for verifying the functionality of a RAM memory in the combined device of Komoike and Kim, since the test patterns that are generated with the conventional state machine based ABIST units are still available, as well as an assortment of new programmable test patterns, thus providing design flexibility.

Response to Arguments

Applicant's arguments, filed with the Amendment 6/1/2005 with respect to the prior Office Action rejections of claims 1-22 under 35 U.S.C. 102 and 103, have been fully considered and are persuasive. Therefore, the rejection has been withdrawn.

However, upon further consideration, a new grounds of rejection is made in view of Claims as being unpatentable over Komoike (U.S. Patent N0. 6,094,736) in view of Kim et al. (U.S. Patent No. 6,148,426), over Komoike (U.S. Patent N0. 6,094,736) in view of Beauchesne et al. (U.S. Patent No. 4,481,627), and over Komoike (U.S. Patent N0. 6,094,736) in view of Kim et al. (U.S. Patent No. 6,148,426) and further in view of Rapoport (U.S. Patent No. 5,557,619), as set forth in the present Office Action.

The Examiner agrees with the Applicant's argument that Ayers fails to disclose a data and address generator internal to the integrated circuit, as amended.

However, under new grounds of rejection, Kim discloses a data generator 103 and an address generator 105 internal to a semiconductor device using a SRAM BIST circuit 100 implemented in connection with memory test processes, Figure 1. The data generator 103 generates data to be written to the memory block 200 under test (i.e., the SRAM) and also generates comparison data. The address generator 105 generates the addresses of the locations of the memory block 200 being tested.

Applicant's arguments with respect to claims 1-25 are moot in view of the new grounds of rejection.

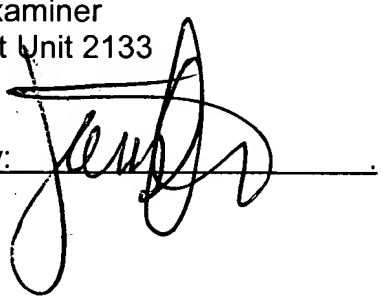
Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to JAMES C. KERVEROS whose telephone number is (571) 272-3824. The examiner can normally be reached on 9:00 AM TO 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on (571) 272-3819. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JAMES C KERVEROS
Examiner
Art Unit 2133

By: 

Randolph Building, 401 Dulany Street,
Alexandria, VA 22314
Tel: (571) 272-3824, Fax: (571) 273-3824
james.kerveros@uspto.gov

Date: 27 July 2005
Office Action: Non-Final Rejection